REMARKS

This paper is being provided in response to the Final Office Action dated May 31, 2006, for the above-referenced application. In this response, Applicant has made minor amendments to claims 1 and 6 to clarify that language therein. Further, Applicants respectfully request consideration of the following remarks.

The rejection of Claims 1 and 6 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,545,575 to Cheng et al. (hereinafter "Cheng") is hereby traversed and reconsideration is respectfully requested.

Independent claim 1 recites a semiconductor device that includes a semiconductor substrate and an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated. A gate electrode is formed on the semiconductor substrate. The gate electrode and the insulating film define at least one lightly doped first drain and source diffusion layer. At least one sidewall covers said gate electrode therewith. At least one heavily doped second drain and source diffusion layer is formed at a surface of the semiconductor substrate around the gate electrode. The at least one lightly doped first drain and source diffusion layer contacts the at least one heavily doped second drain and source diffusion layer on at least a bottom and a lateral side. The at least one sidewall has connected thereto a sidewall offset extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one of regions below which the at least one heavily doped second drain and source diffusion layer is to be formed. The sidewall offset has a lateral dimension extending along a lateral surface of a gate oxide film on which the gate electrode is formed by an amount that is greater than a thickness of the sidewall. The at least one

lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the at least one heavily doped second drain and source diffusion layer extends below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along the surface of the semiconductor substrate. The at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer.

Independent claim 6 recites a semiconductor device including a semiconductor substrate and an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricate. A gate electrode is formed on the semiconductor substrate. The gate electrode and the insulating film define at least one lightly doped first drain and source diffusion layer. At least one sidewall covers the gate electrode therewith. At least one heavily doped second drain and source diffusion layer is formed at a surface of said semiconductor substrate around the gate electrode. The at least one lightly doped first drain and source diffusion layer contacts the at least one heavily doped second drain and source diffusion layer on at least a bottom and a lateral side. The at least one sidewall has connected thereto a sidewall offset extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one of regions below which the at least one heavily doped second drain and source diffusion layer is formed. The sidewall offset extends along a lateral surface of a gate oxide film on which the gate electrode is formed by an amount that is greater than a thickness of said sidewall. Low-resistive wiring layers are formed at surfaces of the drain and source diffusion layers. The low-resistive wiring layers are located

outwardly beyond a peripheral edge of at least one of the sidewall and the sidewall offset in the at least one of said drain and source diffusion layer. The at least one lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the at least one heavily doped second drain and source diffusion layer extend below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along the surface of the semiconductor substrate. The at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer.

The Cheng reference discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the source/drain diffusion regions to form silicide 64. (See Abstract; col. 5, lines 39-67; and Figures 7 and 15 of Cheng).

Concerning Cheng, the Office Action purports to refute Applicant's entire arguments in the prior Response by stating (on page 6, last paragraph) with respect to Cheng that: "Sidewall 66 in figure 15 terminates and has an outer edge at layer 67 or 73." Applicants point that that sidewall 66' terminates *inside* layers 67' or 73' and not at an edge of layer 67' or 73', as is clearly shown in Figure 15 (also, see Figure 10 of Cheng). Further, Applicant recites a heavily doped source or drain diffusion layer that extends below the sidewall offset. The layers 67 (67') or 73 (73') of Cheng cited by the Office Action do not extend below a sidewall offset, but rather are positioned above a substrate surface. Moreover, Applicant recites the feature in which *an*

outer lateral dimension of the heavily doped source or drain diffusion layer is at approximately a an outer edge of the sidewall offset in a vertical direction. As noted above, the layer 67 (67') or 73 (73') cited in the Office Action do not disclose the relative positioning of the sidewall offset and heavily doped source or drain diffusion layer as is recited by Applicant. Accordingly, Applicant submits that the above-noted statements in the Office Action comparing Cheng's Figure 15 to Applicant's claimed invention does not accurately reflect what is shown in Cheng's Figure 15.

Applicant's independent claims 1 and 6 recite a semiconductor device including at least one heavily doped second drain and source diffusion layer extending below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along said surface of said semiconductor substrate and that has an outer lateral dimension along the surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer. For purposes of example, Applicant refers to Figure 3 of Applicant's originally-filed specification which includes a gate electrode 52 having a sidewall 53 and a sidewall offset 54. Heavily doped source and drain diffusion layers 65 and 66 are illustrated as having an outer lateral dimension in a vertical direction and the outer edge of the sidewall 54 is illustrated as having an outer edge which is approximately at the outer lateral dimension of diffusion layers 65 and 66 and are shown spaced outwardly away from the edge of the gate electrode in a direction along the surface of the semiconductor substrate.

Applicant refers to the remarks above concerning the statements in the Office Action about Cheng's Figure 15 with respect to Applicant's claimed invention. Further, Applicant

points out that Cheng includes lightly doped source and drain regions 77' and 78', heavily doped source and drain diffusion layers 82' and 84' and the sidewall 66'. The sidewall 66' is illustrated as having an outer edge which extends further along the substrate surface than the portions 82' and 84' located at the substrate surface. Moreover, as discussed above, sidewall 66' extends into layers 67' and 73' disposed above the substrate surface. Figure 7 of Cheng similarly illustrates sidewall 66 extending further along the substrate surface than the portions 57 and 58 and also discloses sidewall extending into layers 67 and 73 disposed above the substrate surface.

Accordingly, Applicant respectfully submits that Cheng does not teach or fairly suggest at least the above-noted features as claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,316,977 to Kunishima et al. (hereinafter "Kunishima") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent Claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 5, 7, 11, 21 and 23 depend therefrom.

Kunishima discloses a method of manufacturing a semiconductor device comprising metal silicide. The Kunishima reference is cited by the Office Action as disclosing a silicide layer comprising titanium silicide, using a semiconductor device as a CMOS device, and a sidewall entirely covering the gate electrode.

Applicant respectfully submits that Kunishima does not overcome the above-noted deficiencies of the Cheng reference with respect to Applicant's claimed invention. Kunishima does not disclose the configuration of a sidewall offset and heavily doped source and drain diffusion layers as set forth in Applicant's claims. As seen in Figure 3B of Kunishima, Kunishima discloses only a shallow diffusion layer 17, does not disclose a sidewall offset, and accordingly, does not disclose or suggest the above-referenced recited features of Claims 1 and 6 regarding an outer lateral dimension of a heavily doped second source and drain diffusion layer and an outer edge of a sidewall offset. Accordingly, Applicant respectfully submits that neither Kunishima nor Cheng, taken alone or in any combination, teach or fairly suggest the above noted features as claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 20 and 22 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,439,835 to Gonzalez (hereinafter "Gonzalez") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 20 and 22 depend therefrom.

Applicant respectfully submits that Gonzalez does not overcome the above-noted deficiencies of Cheng with respect to the Applicant's presently claimed invention. Gonzalez discloses a gate electrode, sidewall and sidewall offset and drain and source regions (see, for

example, Figures 7-9 of Gonzalez), but the sidewall of Gonzalez below which are positioned multiple drain and source regions does not include a sidewall offset. Further, as seen for example in Figures 8 and 9, Gonzalez's N-implant region 81 has a portion under a sidewall; however the region disposed at the semiconductor substrate surface further extends laterally along the substrate surface beyond the sidewall. Thus, Gonzalez neither discloses nor suggests the above-referenced recited features of Claims 1 and 6 regarding an outer lateral dimension of a heavily doped second source and drain diffusion layer and an outer edge of a sidewall offset. Accordingly, Applicant respectfully submits that Gonzalez and Cheng, taken alone or in any combination, do not teach or suggest at least the above features as claimed by Applicant and thus Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,
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Date: August 25, 2006

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